



DESIGN OF HIGH ORDER DATA CONSTRUCTION BASED SORTING NETWORK USING COUNTER AND COMPRESSOR

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ABSTRACT Parallel counters are enter components in numerous number juggling circuits, particularly quick multipliers. The summation of multiple operands in parallel forms part of the critical path in various digital signal processing units. To speed up the summation, high compression ratio counters and compressors are necessary. In this article, we present a novel method of fast saturated binary counters and exact/approximate (4:2) compressors based on the sorting network. The inputs of the counter are asymmetrically divided into two groups and fed into sorting networks to generate reordered sequences, which can be solely represented by one-hot code sequences. Between the reordered sequence and the one-hot code sequence, three special Boolean equations are established, which can significantly simplify the output Boolean expressions of the counter. Further, this project is enhanced by using parallel sorting algorithms for finding/ sorting M largest values from N inputs and then design scalable architectures based on proposed algorithms. For finding the largest values the iterative sorting techniques also proposed. Bitonic Sorting Is one type of efficient such algorithm for implementing with optimised parameters.

Keywords: *Digital Counter, approximate (4:2) compressors, Sorting, asymmetric, Digital signal processing, Arithmetic Logic Unit.*

INTRODUCTION: Energy minimization is major requirements in almost any electronic systems, especially the portable ones such as smart phones, tablets, and different gadgets. It is extremely desired to attain this minimization with minimal performance (speed) penalty [1]. Digital signal processing (DSP) blocks are most wanted in transportable components for realizing various multimedia applications. The computational core of these blocks is the ALU where the multiplications and additions are the major part [6]. The multiplications plays foremost operation in the processing elements which can leads to high consumption of energy and power. Many of the DSP cores implement image and video processing algorithms where final outputs are either images or videos prepared for human consumptions. It facilitates to go for approximations for improving the speed and energy in the arithmetic circuits. This originates from the limited perceptual abilities in observing an image or a video for human beings. In addition to the image and video processing applications, there are other areas where the exactness of the arithmetic operations is not critical to the functionality of the system (see [2],[3]). Approximate computing provides an accuracy, speed and power/energy consumption. The advantage of approximate multiplier reduces the error rate and gain high speed. For correcting the division error compare operation and a memory look up is required

for the each operand is required which increases the time delay for entire multiplication process [4]. At various level of abstraction including circuit, logic and architecture levels the approximation is processed [5]. In the category for approximation methods in function, a number of approximating arithmetic building blocks, such as adders and multipliers, at different design levels have been suggested in various structures [6],[7]. Broken array multiplier was designed for efficient VLSI implementation [8].

LITERATURE SURVEY: A traditional method to reduce the aging effects is overdesign which includes techniques like guard-banding and gate oversizing. This approach can be area and power inefficient [8]. To avoid this problem, an NBTI-aware technology mapping technique was proposed in [7] which guarantee the performance of the circuit during its lifetime. Another technique was an NBTI-aware sleep transistor in [3] which improve the lifetime stability of the power gated circuits under considerations. A joint logic restructuring and pin reordering method in [6] is based on detecting functional symmetries and transistor stacking effects. This approach is an NBTI optimization method that considered path sensitization. Dynamic voltage scaling and body-biasing techniques were proposed in [4] and [5] to reduce power or extend circuit life. These techniques require circuit modification or do not provide optimization of specific circuits. Every gate in any VLSI circuit has its own delay which reduces the performance of the chip. Traditional circuits use critical path delay as the overall circuit clock cycle in order to perform correctly. However, in many worst-case designs, the probability that the critical path delay is activated is low. In such cases, the strategy of minimizing the worst-case conditions may lead to inefficient designs. For noncritical path, using the critical path delay as the overall cycle period will result in significant timing waste. Hence, the variable latency design was proposed to reduce the timing waste of traditional circuits. A short path activation function algorithm was proposed in [16] to improve the accuracy of the hold logic and to optimize the performance of the variable-latency circuit. An instruction scheduling algorithm was proposed in [17] to schedule the operations on nonuniform latency functional units and improve the performance of Very Long Instruction Word processors. In [18], a variable-latency pipelined multiplier architecture with a Booth algorithm was proposed. In [19], process-variation tolerant architecture for arithmetic units was proposed, where the effect of process-variation is considered to increase the circuit yield. In addition, the critical paths are divided into two shorter paths that could be unequal and the clock cycle is set to the delay of the longer one. These research designs were able to reduce the timing waste of traditional circuits to improve performance, but they did not consider the aging effect and could not adjust themselves during the runtime.

SORTING: A sorting network is a collection of interconnected compare-and-exchange (CAE) block. Sorting networks consist of comparators, which are in fact hardware implementations of the CE operation. A comparator has two inputs and two outputs. Depending on the sense of ordering, comparators can be of two kinds as shown in figure 1 (a), (b).

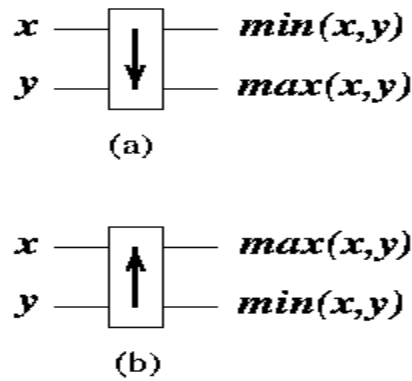


Fig1: Basic Sorting Unit

Sorting is any process of arranging items according to a certain sequence or in different sets, and therefore, it has two common, yet distinct meanings:

PARALLEL SORTING NETWORKS A sorting network is a collection of interconnected compare-and-exchange (CAE) blocks that guides a parallel set of inputs to a parallel set of outputs in sorted order. Each CAE block has two inputs and two outputs. If the input values are already in order, they are directed to the corresponding outputs; otherwise, they are swapped. There are two types of CAE blocks, called increasing and decreasing CAE blocks, used in hardware-based sorting

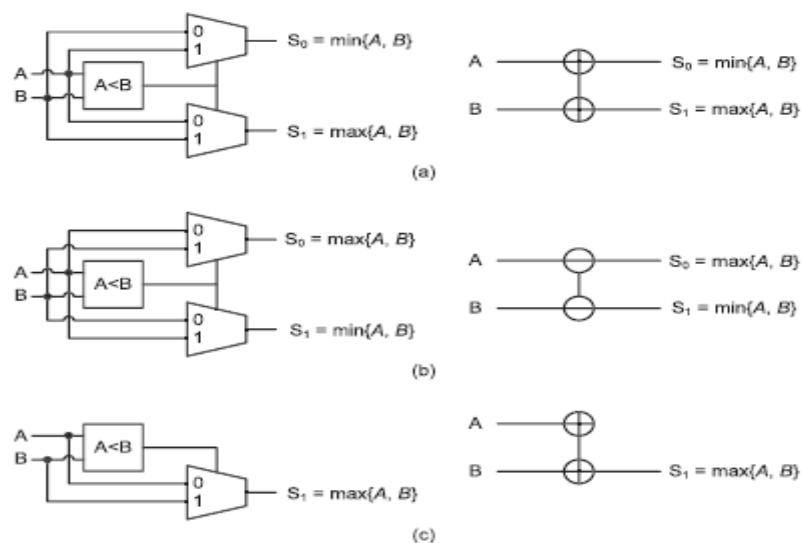


Fig:2 parallel sorting units

units. Fig.2 shows the high-level implementations (left) and schematic symbols (right) for three building blocks used in previous sorting units and in our designs. A decreasing CAE block, shown in Fig. 2b, outputs its inputs in descending order. Decreasing and increasing CAE blocks are identical, except for their wiring. Each CAE block contains a comparator and two multiplexers. We also define Max units which are used in our designs. A Max unit, shown in Fig. 1c, takes two inputs and returns the larger input. Note that the \oplus and \ominus symbols determine the type of the block in Fig. 2. A sorting network usually consists of a series of stages in which each stage contains a number

of CAE blocks that operate in parallel. The latency of a sorting network is proportional to its depth (the number of consecutive CAE blocks). Two popular parallel sorting networks that currently have the lowest known latency for hardware implementation are the bitonic and odd-even merge sorting networks proposed by Batcher [25]. The structure of a sorting network is fixed, regardless of the value of the numbers being sorted and the results of the comparisons. Sorting networks are a common solution for hardware-based sorting. Their parallel nature allows them to perform sorting much faster than the $O(N \log N)$ time achievable by the fastest sequential software-based sorting algorithms. A sorting network may also be pipelined to further increase throughput.

EXISTING TECHNIQUE:

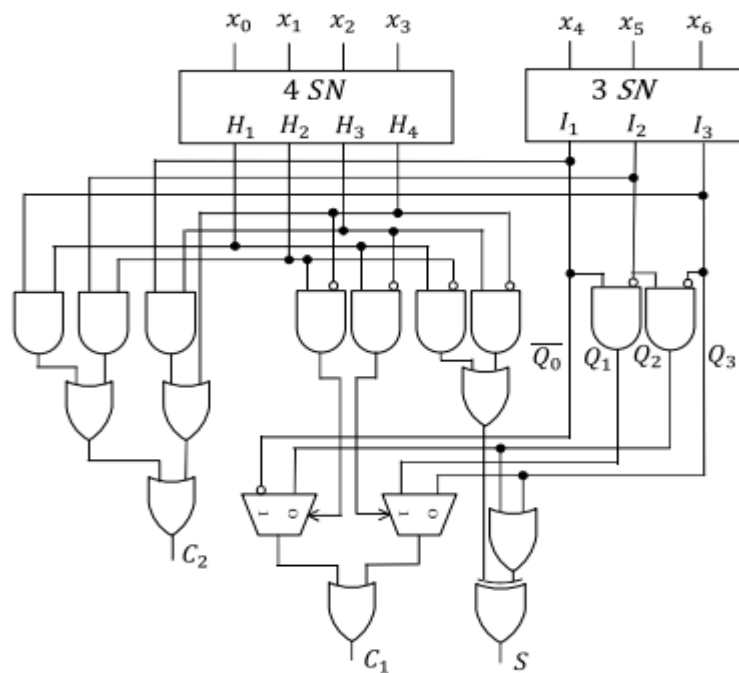


Fig:3 Overall (7,3) counter circuit

The whole architecture is shown in above Fig. It is obvious that the paths from sequences H and I to C2, C1, and S are almost independent. Increases the parallelism of the circuit. However, as will be discussed later, the area of the proposed design will not increase with the parallelism.

IMPLEMENTATION: First, as shown in above Fig. due to the fact that “1” is bigger than “0,” all the “1”s are at the top of the sequence if there exist “1”s, and all the “0”s are at the bottom of the sequence if there exist “0”s. If there exist both “1”s and “0”s, there must be a position in the reordered sequence where there is the junction of “1” and “0.” If there are only “1”s or “0”s, we can manage the sequence by padding fixed one bit “1” at the top and one bit “0” at the bottom of the reordered sequence to make sure that 0,1-junction always exists. Second, the reordered sequence has the same total number of “1”s and “0”s as the original sequence (the inputs of two sorting networks). Although the padded “1” would influence the total number of “1”s in the padded sequence, it is fixed, so we ignore it while counting.

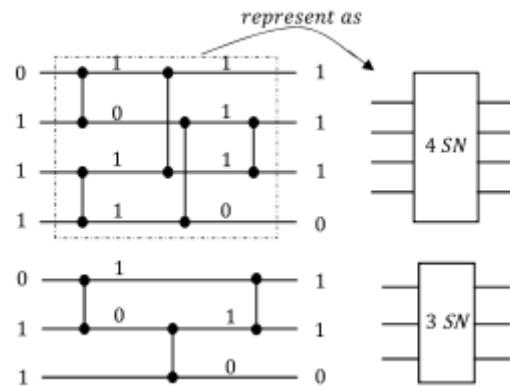


Fig.4 Three- and four-way sorting networks.

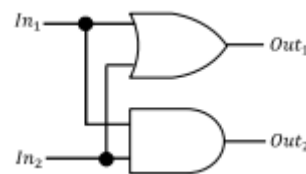


Fig.5 Two-input binary sorter

we give an input example: sequence [0, 1, 1, 1] represents the input of four-way sorting network (4 SN), and sequence [0, 1, 1] represents the input of three-way sorting network (3 SN). For both 4 SN and 3 SN, the input sequences are reordered in the form of the larger number at the top and the smaller number at the bottom after three layers of sorter.

ONE-HOT CODE GENERATION

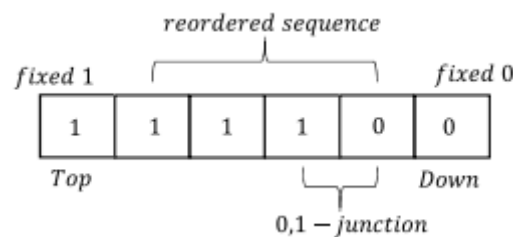


Fig.6 Definition of a sequence.

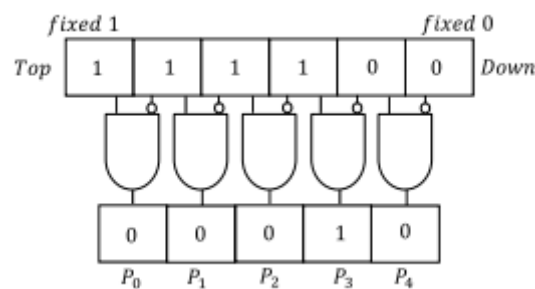


Fig. 7 One-hot code generation circuit.

1) Asymmetric Prereorder: Both three- and four-way sorting networks require three layers of binary sorter (the two binary sorters on the same layer in fourway sorting network can be calculated in parallel). Each layer of binary sorters consumes one basic two-input logical gate layer, as shown in Fig. 3. This means that the time consumed by the three- and four-way sorting networks is almost the same. Based on this, we divide the seven inputs of a (7,3) counter into two parts. One part contains 4 bits, while the other contains 3 bits.

2) Find 0,1-Junction and One-Hot Code Sequence: The 0,1-junction can solely represent the reordered sequence under the promise of the extended fixed “0” and “1.” Notice that the position of the 0,1-junction must be 1,0 from left to right. Therefore, we still utilize the fourway sorting network as an example, and then, This structure uses a Boolean expression (AB) to obtain a new sequence P0–P4. Because there is one and only one 0,1-junction in the reordered and extended sequence, there is one and only one “1” in sequence P0–P4. This means that sequence P0–P4 is one-hot code that satisfies (“|” represents

TRUTH TABLE OF (7,3) COUNTER OUTPUTS

Num	C_2	C_1	S	Num	C_2	C_1	S
0	0	0	0	4	1	0	0
1	0	0	1	5	1	0	1
2	0	1	0	6	1	1	0
3	0	1	1	7	1	1	1

“OR” and “&” represents “AND”) $P_0|P_1|P_2|P_3|P_4 = 1$. (1) If the sequence elements (P0–P4) are randomly divided into two groups, such as P0, P2, and P4 as group 1 and P1 and P3 as group 2, then, because of one and only one “1” in the sequence, we have $P_0|P_2|P_4 = P_3|P_1$. (2) All results of random separation satisfy this rule. We also apply the same method on the three-way sorting network’s output sequence and get the one-hot code sequence Q0–Q3. This sequence also satisfies the rule above.

we have two sequences P and Q. $P_0 = 1$ means that there is no “1” in the input sequence of four-way sorting network, $P_1 = 1$ represents one “1” in it, and $P_i = 1$ represents i “1”s in it and so is the sequence Q. Here are some symbol conventions. The outputs of (7,3) counter are denoted as C_2 , C_1 , and S , and C_2 has the most significant weight, while S has the lowest weight. Table I shows the total numbers of “1”s (“Num” column in the table) in the input 7 bits corresponding to outputs, i.e., $\text{Num} = 22C_2 + 21C_1 + 20S$. The sequence output from four-way sorting network is denoted as sequence H, including H1–H4 from left to right in Fig. 4. The sequence output from three-way sorting network is denoted as sequence I, including I1–I3 from left to right. According to Table I, we know that at least four “1”s are in the input sequence of the (7,3) counter when $C_2 = 1$. As discussed before, $P_4 = 1$ means that four “1”s are in sequence H (also in the input sequence of 4 SN because sorting network has no effect on total number of “1”s), and $Q_0 = 1$ means that no “1” is in sequence I. Thus, $P_4 \& Q_0 = 1$ means that there are totally $4 + 0 = 4$ “1”s in the input 7 bits. As a result of this type of representation, C_2 is equal to 1 when the summation of subscripts of P and Q is no less than 4. In this way, C_2 can be expressed as

$$C_2 = (P_4 \& (Q_0|Q_1|Q_2|Q_3))|(P_3 \& (Q_1|Q_2|Q_3))| \\ (P_2 \& (Q_2|Q_3))|(P_1 \& Q_3). \quad (3)$$

Notice that the sequence Q , with the same method in (2), satisfies

$$Q_0|Q_1|Q_2|Q_3 = 1 \quad (4)$$

$$Q_1|Q_2|Q_3 = \overline{Q_0}. \quad (5)$$

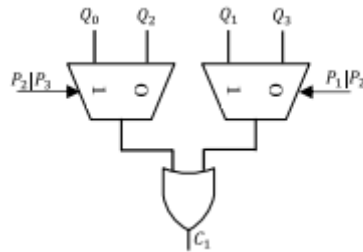


Fig.8 C1 generating circuit.

HIGHER COMPRESSION RATIO COUNTERS:

CONSTRUCT (15,4) COUNTER

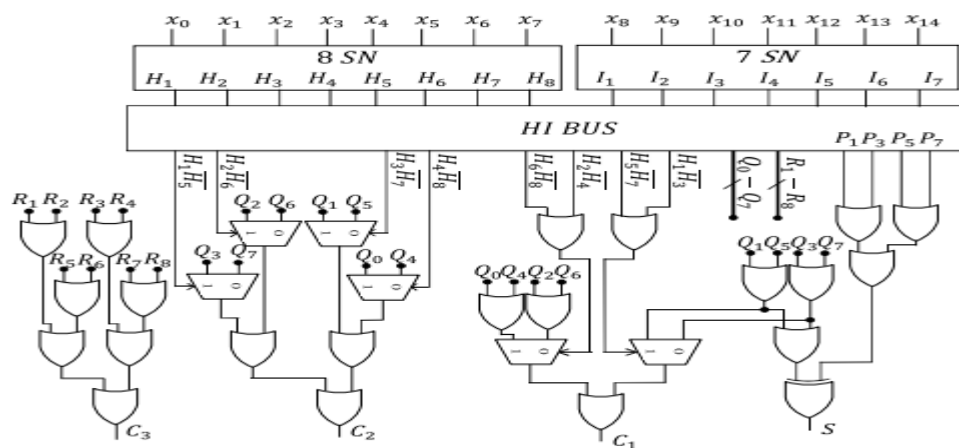


Fig.9 Overall (15,4) counter circuit

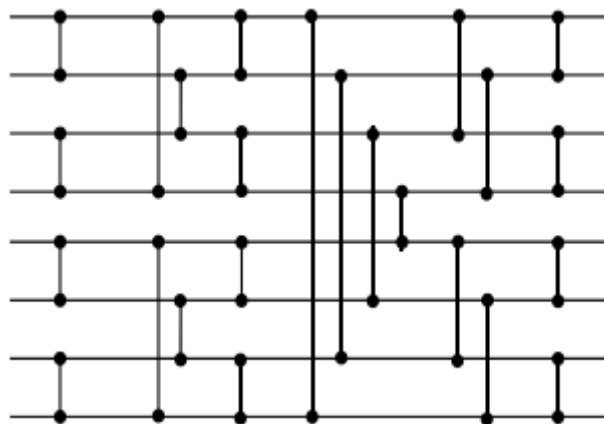


Fig10 Eight-way sorting network.

Seven- and Eight-Way Sorting Networks: Fig. shows an eight-way sorting network [14]. This sorting network consumes six layers of basic logic gates to output the result. Removing one bit from the eight-way sorting network can obtain a seven-way sorting network that also consumes six layers of basic logic gates.

$$Q_0|Q_2|Q_4|Q_6 = \overline{Q_1|Q_3|Q_5|Q_7}$$

$$P_0|P_2|P_4|P_6|P_8 = \overline{P_1|P_3|P_4|P_5|P_7}$$

$$I_i = I_i|I_{i+j},$$

$$(i = 0, 1, \dots, 6, 7; j \geq 0; i + j \leq 8)$$

TRUTH TABLE OF (15,4) COUNTER OUTPUT

TRUTH TABLE OF (15,4) COUNTER OUTPUTS									
Num	C ₃	C ₂	C ₁	S	Num	C ₃	C ₂	C ₁	S
0	0	0	0	0	8	1	0	0	0
1	0	0	0	1	9	1	0	0	1
2	0	0	1	0	10	1	0	1	0
3	0	0	1	1	11	1	0	1	1
4	0	1	0	0	12	1	1	0	0
5	0	1	0	1	13	1	1	0	1
6	0	1	1	0	14	1	1	1	0
7	0	1	1	1	15	1	1	1	1

PROPOSED TECHNIQUE:

BITONIC SORTING: Bitonic sort is one of the fastest sorting networks. A sorting network is a special kind of sorting algorithm, where the sequence of comparisons is not data-dependent.

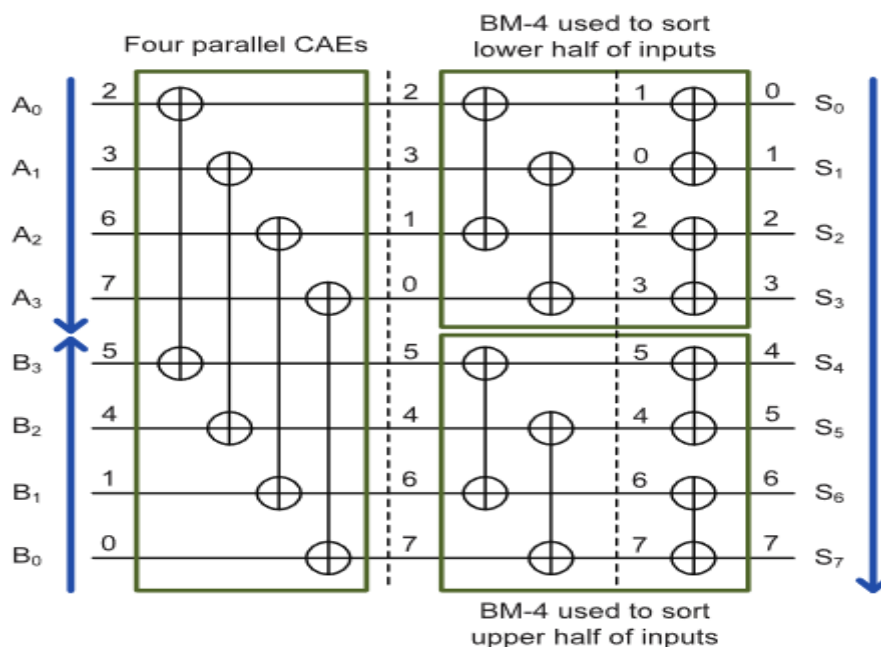


Fig.11 An increasing 8-input bitonic merging unit

Each box performs the same operation as a blue box, but with the sort in the opposite direction. So, each green box could be replaced by a blue box followed by a crossover where all the wires move to the opposite position. This would allow all the arrows to point the same direction, but would prevent the horizontal lines from being straight. However, a similar crossover could be placed to the right of the bottom half of the outputs from any red block, and the sort would still work correctly, because the reverse of a bitonic sequence is still bitonic. If a red box then has a crossover before and after it, it can be rearranged internally so the two crossovers cancel, so the wires become straight again. Therefore, the following diagram is equivalent to the one above, where each green box has become a blue plus a crossover, and each orange box is a red box that absorbed two such crossovers.

RESULTS:

In the current system, the (6,3) and (7,3) Counters have a symmetrical number of inputs. This design has both full and half adders. There is a longer delay and a bigger amount of circuit area used by the increased number of XOR gates. Because of the increased number of XOR gates, the circuit's hardware complexity and power consumption are both high. The suggested counters use a sorting network to arrange the (7,3) and (15,4) counts in symmetrical order. Using this new design would reduce the number of full and half adders required. Because there are no XOR gates in these counters, the latency is less and the amount of space used up by the circuit is reduced. The device uses a little amount of electricity.

The cable is used to link the counter design schematic's needed connections, as illustrated in fig.

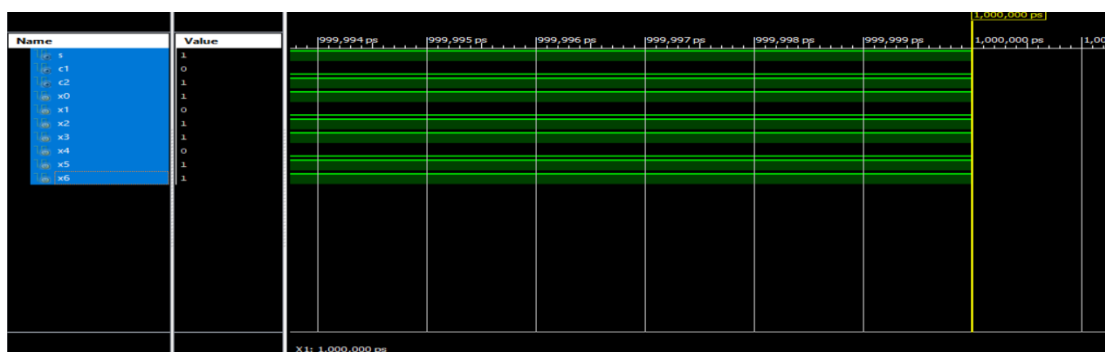


Fig: (7,3) Output waveform

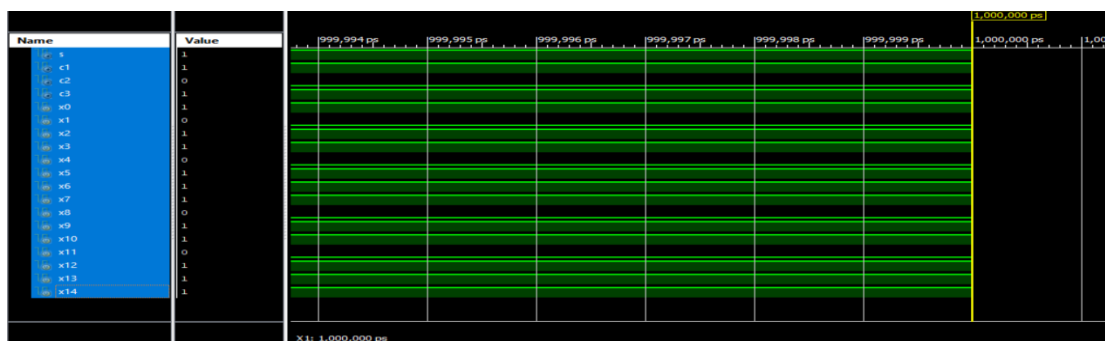


Fig: (15, 4) counter Simulation result

**COMPARISON TABLE OF EXISTING SYSTEM WITH PROPOSED
SYSTEM:**

S/no	Design	Area (no.of.LUT's)	Power (W)	Delay (ns)
1	Symmetric stacking (11)	8	0.081	1.8
2	Proposed (7,3) Counter	3	0.042	1.728
3	Parallel (15,4) Counter (12)	15	0.095	4.1
4	Proposed (15,4) Counter	13	0.042	4.061

CONCLUSION AND FUTURE SCOPE: In this paper, a plan strategy for region viable and speed effective counter is planned and reproduced. A twofold counter in view of a novel symmetric piece Aggregate and convey computation approach is proposed. In this process, a new counter design method based on a sorting network is proposed, and we construct (7,3), (15,4) counters based on this biotonic sorting method. Proposed counters are more flexible than existing designs because it achieves less delay when the speed is critical and performs in better in ADP. The image, videos and the clarity of videos can be checked by using approximate multipliers. And that are tired to match the clarity of the exact multipliers. For faster multiplication we have use Brent Kung Adder to reduce area and to increase speed we can use Kogge Stone Adder.

REFERENCE: [1] Wen-Chang Yeh and Chein-Wei Jen, "High-speed Booth encoded parallel multiplier design," IEEE Trans. on Computers, vol. 49, issue 7, pp. 692-701, July 2000.

[2] Jung-Yup Kang and Jean-Luc Gaudiot, "A simple high-speed multiplier design," IEEE Trans. on Computers, vol. 55, issue 10, Oct. pp. 1253-1258, 2006.

[3] Shiann-Rong Kuang, Jiun-Ping Wang and Cang-Yuan Guo, "Modified Booth multipliers with a regular partial product array," IEEE Trans. on Circuit and Systems, vol.56, Issue 5, pp. 404-408, May 2009.

[4] Li-rong Wang, Shyh-Jye Jou and Chung-Len Lee, "A well-structured modified Booth multiplier design," Proc. of IEEE VLSI-DAT, pp. 85-88, April 2008.

[5] A. A. Khatibzadeh, K. Raahemifar and M. Ahmadi, "A 1.8V 1.1GHz Novel Digital Multiplier," Proc. of IEEE CCECE, pp. 686-689, May 2005.

- [6] S. Hus, V. Venkatraman, S. Mathew, H. Kaul, M. Anders, S. Dighe, W. Burleson and R. Krishnamurthy, "A 2GHZ 13.6mW 12x9b multiplier for energy efficient FFT accelerators," Proc. of IEEE ESSCIRC, pp. 199-202, Sept. 2005.
- [7] Hwang-Cherng Chow and I-Chyn Wey, "A 3.3V 1GHz high speed pipelined Booth multiplier," Proc. of IEEE ISCAS, vol. 1, pp. 457-460, May 2002.
- [8] M. Aguirre-Hernandez and M. Linarsé-Aranda, "Energy-efficient high-speed CMOS pipelined multiplier," Proc. of IEEE CCE, pp. 460-464, Nov. 2008.
- [9] Yung-chin Liang, Ching-ji Huang and Wei-bin Yang, "A 320-MHz 8bit x 8bit pipelined multiplier in ultra-low supply voltage," Proc. of IEEE A-SSCC, pp. 73-76, Nov. 2008.
- [10] S. B. Tatapudi and J. G. Delgado-Frias, "Designing pipelined systems with a clock period approaching pipeline register delay," Proc. of IEEE MWSCAS, vol. 1, pp. 871-874, Aug. 2005.
- [11] A. D. Booth, "A signed binary multiplication technique," Quarterly J. Mechanical and Applied Math, vol. 4, pp.236-240, 1951.
- [12] M. D. Ercegovac and T. Lang, *Digital Arithmetic*, Morgan Kaufmann Publishers, Los Altos, CA 94022, USA, 2003.
- [13] C. S. Wallace, "A suggestion for a fast multiplier," IEEE Trans. On Computers, vol. BC13, pp. 14-17, Feb. 1964.
- [14] M.D. Ercegovac et al., "Fast Multiplication without Carry- Propagate Addition," IEEE Trans. Computers, vol. 39, no. 11, Nov. 1990.
- [15] R.K. Kolagotla et al., "VLSI Implementation of a 200-Mhz 16 _ 16 Left-to-Right Carry-Free Multiplier in 0.35_μm CMOS Technology for Next-Generation DSPs," Proc. IEEE 1997 Custom Integrated Circuits Conf., pp. 469-472, 1997.
- [16] P.F. Stelling and V.G. Oklobdzija, "Optimal Designs for Multipliers and Multiply-Accumulators," Proc. 15th IMACS WorldCongress Scientific Computation, Modeling, and Applied Math., A. Sydow, ed., pp. 739-744, Aug. 1997.
- [17] Passport 0.35 micron, 3.3 volt, Optimum Silicon SC Library, CB35OS142, Avant! Corporation, Mar. 1998.
- [18] G. Goto et al., "A 4.1ns compact 54 _ 54-b Multiplier Utilizing Sign-Select Booth Encoders," IEEE J. Solid-State Circuits, vol. 32, no. 11, pp. 1,676-1,682, Nov. 1997.
- [19] G. Goto et al., "A 54 _ 54-b Regularly Structured Tree Multiplier," IEEE J. Solid-State Circuits, vol. 27, no. 9, Sept. 1992.
- [20] R. Fried, "Minimizing Energy Dissipation in High-Speed Multipliers," Proc. 1997 Int'l Symp. Low Power Electronics and Design, pp. 214-219, 1997.
- [21] N.H.E. Weste and K. Eshraghian, Principles of CMOS VLSI Design: A Systems Perspective, second ed., chapter 8, p. 520. Addison Wesley, 1993.
- [22] J. Fadavi-Ardekani, "M_N Booth Encoded Multiplier Generator Using Optimized Wallace Trees," IEEE Trans. VLSI Systems, vol. 1, no. 2, June 1993.

- [23] A.A. Farooqui et al., ^aGeneral Data-Path Organization of a MAC Unit for VLSI Implementation of DSP Processors,^o Proc. 1998 IEEE Int'l Symp. Circuits and Systems, vol. 2, pp. 260-263, 1998.
- [24] K. Hwang, Computer Arithmetic: Principles, Architecture, and Design, chapter 3, p. 81. John Wiley & Sons, 1976.
- [25] K.H. Cheng et al., ^aThe Improvement of Conditional Sum Adder for Low Power Applications,^o Proc. 11th Ann. IEEE Int'l ASICConf., pp. 131-134, 1998.